FIG. 1A

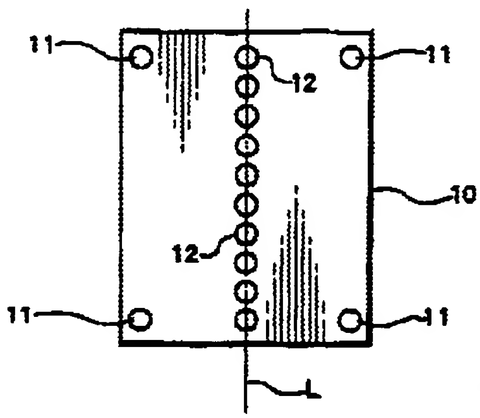


FIG. 1B

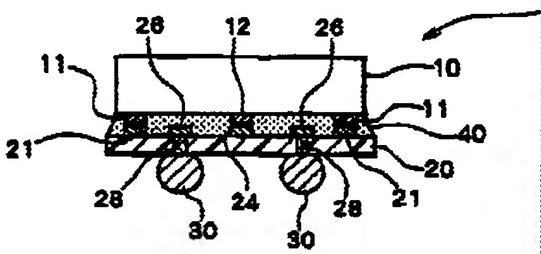
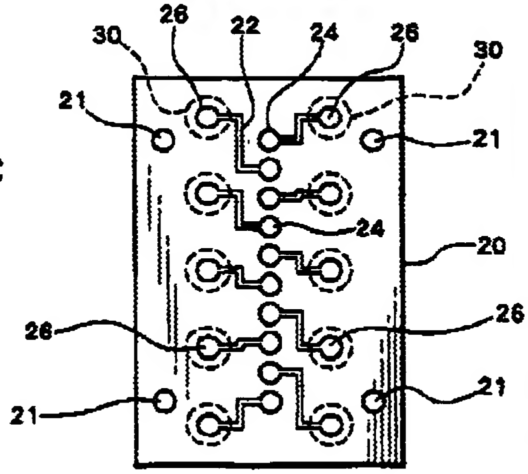


FIG. 1C



(12) United States Patent
Hashimoto

(10) Patent No.: US 6,410,366 B1
(45) Date of Patent: Jun. 25, 2002

(54) SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF, CIRCUIT BOARD AND ELECTRONIC EQUIPMENT

(75) Inventor: Nobuaki Hashimoto, Suwa (JP)

(73) Assignee: Seiko Epson Corporation, Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/555,155

(22) PCT Filed: Sep. 3, 1999

(86) PCT No.: PCT/JP99/04785

§ 371 (c)(1), (2), (4) Date: May 25, 2000

(87) PCT Pub. No.: WO00/19515

PCT Pub. Date: Apr. 6, 2000

(30) Foreign Application Priority Data

Sep. 30, 1998 (JP) 10-292033

(51) Int. Cl.[7] H01L 23/64; H01L 21/45; H01L 21/50; H01L 23/48; H01L 23/12; H01L 29/40; H05K 1/00; H05K 1/18; H05K 7/02; H05K 7/06; H05K 7/08; H05K 7/10; H05K 7/12

(52) U.S. Cl. 438/125; 438/108; 257/778; 361/746; 361/760; 361/770

(58) Field of Search 438/106, 125; 257/778; 361/748, 760, 770

(56) References Cited

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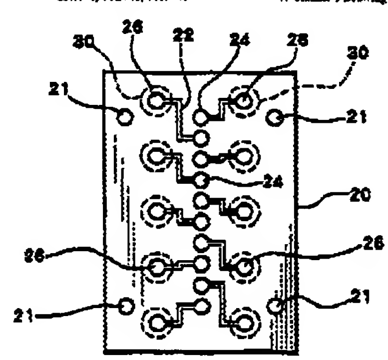
* cited by examiner

Primary Examiner—Tuan H. Nguyen
Assistant Examiner—Necia Barnes
(74) Attorney, Agent, or Firm—Oliff & Berridge PLC

(57) ABSTRACT

A semiconductor device comprising: a semiconductor chip (10) which is subjected to face-down bonding, having a plurality of electrodes (12) aligned on a straight line (L); a substrate (20) on which is formed an interconnect pattern (22) having bonding portions (24) to which the electrodes (12) of the semiconductor chip (10) are connected and lands (26) electrically connected to the bonding portions (24); external electrodes (30) passing through the substrate (20) and connected to the lands (26); and a support formed from bumps (11, 21) provided between the semiconductor chip (10) and substrate (20), wherein the connected electrodes (12) and bonding portions (24) and the support formed by the bumps (11, 21) maintain the semiconductor chip (10) and substrate (20) substantially parallel.

44 Claims, 6 Drawing Sheets



FIGS. 4A to 4C illustrate a third embodiment of a semiconductor device to which the present invention is applied.

FIG. 5 shows a circuit board having mounted this embodiment of the semiconductor device.

FIG. 6 shows an electronic instrument having a circuit board on which is mounted this embodiment of the semiconductor device.

BEST MODE FOR CARRYING OUT THE INVENTION

The present invention is now described in terms of a number of preferred embodiments, with reference to the drawings.

First Embodiment

FIGS. 1A to 1C illustrate a first embodiment of a semiconductor device to which the present invention is applied. It should be noted that FIG. 1A shows the active surface of the semiconductor chip forming a part of the semiconductor device, FIG. 1B is a sectional view of the semiconductor device, and FIG. 1C shows the surface of the substrate, forming a part of the semiconductor device, on which the interconnect pattern is formed. A semiconductor device **1** comprises a semiconductor chip **10** and substrate **20**.

The semiconductor chip **10** is for example a DRAM or synchronous DRAM, and has a plurality of electrodes **12**. The electrodes **12** are disposed concentrated on and around a straight line L. For example, the electrodes **12** can be arranged in a row on the straight line L. The straight line L extends parallel to the longer edges and in the center of the rectangular semiconductor chip **10**, but may equally extend parallel to the shorter edges. The electrodes **12** are commonly of gold formed by plating or wire bonding and tearing out, but may equally be of nickel, solder, or the like.

On the semiconductor chip **10** is provided one or a plurality of bumps **11**. The bumps **11** are provided in positions removed from the straight line L. For example, the bumps **11** may be provided in at least one of the four corners of the semiconductor chip **10**. Alternatively, one or a plurality of bumps **11** may be provided in central portions (portions excluding the corners) of the longer edges parallel to the straight line L of the semiconductor chip **10**. The bumps **11** are preferably formed of an electrically insulating material. The bumps **11** are resilient and of relatively small form such as to be able to be squashed down, and are preferably for example of approximately the same flat shape as the electrodes **12**. When the bumps **11** are formed of the same material as the electrodes **12** in the same process, it is preferable to provide an electrical insulating means by covering with an insulating film, for example. In this case also, it is preferable for the bumps **11** to be of sufficiently small form to be seen as points. The bumps **11** can be formed of approximately the same height as the electrodes **12**, but are not limited thereto. The bumps **11** form a support in combination with bumps **21** formed on the substrate **20**. The bumps **11** may function as electrodes **12** (may form electrical contacts), and may be connected to other interconnect patterns. This is also true similarly of the embodiments described hereafter.

The substrate **20** may be formed of either an organic or an inorganic material, or may equally be a composite structure thereof. As a substrate **20** formed of an organic material may be cited for example a flexible substrate formed of a polyimide resin. As a substrate **20** formed of an inorganic material may be cited for example a ceramic substrate or glass substrate. As a composite structure of organic and inorganic material may be cited for example a glass epoxy

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(12) **United States Patent**
Hashimoto

(10) **Patent No.: US 6,410,366 B1**
(45) **Date of Patent: Jun. 25, 2002**

(54) **SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF, CIRCUIT BOARD AND ELECTRONIC EQUIPMENT**

(75) Inventor: Nobuaki Hashimoto, Suwa (JP)

(73) Assignee: Seiko Epson Corporation, Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/333,139

(22) PCT Filed: Sep. 3, 1999

(86) PCT No.: PCT/JP99/04785

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(2), (4) Date: May 25, 2000

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(30) Foreign Application Priority Data

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(51) Int. Cl.[7] H01L 23/04; H01L 21/48; H01L 21/50; H01L 23/48; H01L 23/12; H01L 29/40; H05K 1/00; H05K 1/18; H05K 7/02; H05K 7/06; H05K 7/08; H05K 9/12

(52) U.S. Cl. 438/125; 438/128; 257/778; 361/748; 361/760; 361/772

(58) Field of Search 438/106, 125; 257/778; 361/748, 760, 770

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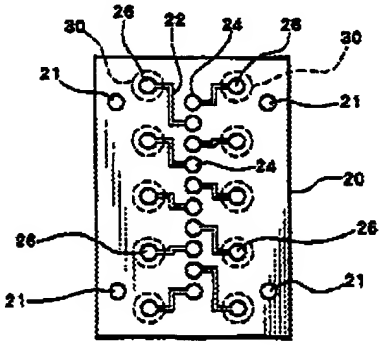
Primary Examiner—Tuan H. Nguyen
Assistant Examiner—Nancy Barnes
(74) *Attorney, Agent, or Firm*—OIPE & Berridge PLC

(57) **ABSTRACT**

A semiconductor device comprising: a semiconductor chip (10) which is adapted to face-down bonding, having a plurality of electrodes (12) aligned on a straight line (L), a substrate (20) on which is formed an interconnect pattern (22) having bonding portions (24) to which the electrodes (12) of the semiconductor chip (10) are connected and leads (26) electrically connected to the bonding portions (24); external electrodes (30) passing through the substrate (20) and connected to the leads (26); and a support formed from bumps (11, 21) provided between the semiconductor chip (10) and substrate (20), wherein the connected electrodes (12) and bonding portions (24) and the support formed by the bumps (11, 21) maintain the semiconductor chip (10) and substrate (20) substantially parallel.

44 Claims, 4 Drawing Sheets



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bonding portions;

(49) a step of subjecting the semiconductor chip to face-down bonding to connect the electrodes to the bonding portions; and

(50) a step of providing at least one support between the semiconductor chip and the substrate, of approximately the same height as the total thickness of the electrodes and the bonding portions.

(51) According to the present invention, a plurality of electrodes are aligned concentrated in the vicinity of a straight line, and the semiconductor chip which would not be stable with the electrodes alone, is maintained parallel to the substrate by the support. Therefore, bonding can be carried out appropriately so that the electrodes and bonding portions are not bent. The lateral sides of the semiconductor chip contacting the interconnect pattern formed on the substrate and making an electrical connection is prevented. Furthermore, bending of the substrate can be prevented.

(52) Since the semiconductor chip is subjected to face-down bonding, the bonding is carried out within the area of the semiconductor chip. Therefore, the area of the substrate can be reduced to the minimum necessary. As a result, the semiconductor device can be made more compact.

(53) (15) In the step of providing a support in this method, the support may be provided beforehand on one of the semiconductor chip and the substrate, and the other of the semiconductor chip and the substrate may be contacted with the support.

(54) (16) In the step of providing a support in this method, the support may be formed by bonding first bumps formed on the semiconductor chip of the same material as the electrodes and distanced from the electrodes and second bumps formed on the substrate of the same material as the interconnect pattern and distanced from the interconnect pattern.

(55) The first bumps can be formed at the same time as the electrodes, and

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US006410366B1

(12) **United States Patent**
Hashimoto

(10) Patent No.: US 6,410,366 B1
(45) Date of Patent: Jun. 25, 2002

(54) SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF, CIRCUIT BOARD AND ELECTRONIC EQUIPMENT

(75) Inventor: Nobuaki Hashimoto, Suwa (JP)
(73) Assignee: Seiko Epson Corporation, Tokyo (JP)

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(21) Appl. No.: 09/353,139
(22) PCT Filed: Sep. 3, 1999
(86) PCT No.: PCT/JP99/04785
§ 371 (c)(1),
(2), (4) Date: May 25, 2000
(87) PCT Pub. No.: WO00/19515
PCT Pub. Date: Apr. 6, 2000

(30) Foreign Application Priority Data
Sep. 22, 1998 (JP) 10-268033

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(52) U.S. Cl. 438/108; 438/125; 257/778; 361/749; 361/760; 361/770
(58) Field of Search 438/108, 125; 257/778; 361/749, 760, 770

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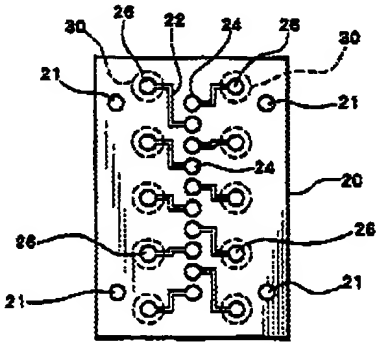
Primary Examiner—Tuan H. Nguyen
Assistant Examiner—Nema Berezny
(74) *Attorney, Agent, or Firm*—Oliff & Berridge PLC

(57) ABSTRACT

A semiconductor device comprising: a semiconductor chip (10) which is subjected to face-down bonding, having a plurality of electrodes (12) aligned on a straight line (L), a substrate (20) on which is formed an interconnect pattern (22) having bonding portions (24) to which the electrodes (12) of the semiconductor chip (10) are connected and leads (26) electrically connected to the bonding portions (24); external electrodes (30) passing through the substrate (20) and connected to the leads (26); and a support formed from bumps (21, 21) provided between the semiconductor chip (10) and substrate (20), wherein the connected electrodes (12) and bonding portions (24) and the support formed by the bumps (21, 21) maintain the semiconductor chip (10) and substrate (20) substantially parallel.

44 Claims, 6 Drawing Sheets



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printed wiring board. To evaluate the connection reliability, the maximum equivalent plastic strain on each bump was calculated by simulation, and sample devices were subjected to a thermal shock test, wherein the sample devices were repeatedly cooled and heated in air, each time cooled at -40.degree. C. for 30 minutes and then heated at +100.degree. C. for 30 minutes.

(39) FIG. 4 is a diagram representing the relationship between the maximum equivalent plastic strain and the bump height, which as observed by simulation with an electronic circuit device comprising a glass-epoxy resin printed wiring board and a chip component of 1608 type (planar size: 1.6.times.0.8 mm). The bumps used in the device subjected to the simulation were beer barrel-shaped ones. That part of each bump which covered the side of the electrode was not taken into consideration in the simulation. As illustrated in FIG. 4, the maximum equivalent plastic strain on the bump decreased as the bump height increased up to 50 .mu.m, and remained almost unchanged as the bump height further increased. In particular, when the bump height was 50 .mu.m or less, the strain was particularly prominent, indicating that the connection between the chip component and the glass-epoxy resin board was not so reliable as desired.

(40) The sample devices subjected to the aforementioned thermal shock test comprises a chip component of 1608 type. To be more specific, four groups of sample devices were made for experimental purpose. The devices of the first group had bumps 5 .mu.m high; the devices of the second group had bumps 60 .mu.m high; the devices of the third group had bumps 70 .mu.m high; and the devices of the fourth group had bumps 90 .mu.m high. The results of the thermal shock test were as is shown in FIG. 5. In FIG. 5, the ratio (%) of all failed samples is plotted on the abscissa, and the number of thermal cycles on the ordinate. The term "failed sample" means a sample device which had the connection resistance increased two or more times as the result of the thermal shock test. As is evident from FIG. 5, the samples of the second, third and

Uchida

US005684677A

s Patent [19]

[11] Patent Number: 5,684,677

[45] Date of Patent: Nov. 4, 1997

CUIT DEVICE

Uchida, Yokohama; Takashi , Tokyo; Miki Mori, a; Masayuki Saito, ; Takaaki Togasaki, a; Yukio Kimiki, Yokohama, an

ki Kabsha Toshiba, Kawasaki,

996

Application Data

38,222, Nov. 17, 1995, abandoned, of Ser. No. 265,102, Jun. 24, 1994,

reign Priority Data

a 5-153150

a 6-077367

..... H05K 7/02; H05K 7/10; H05K 1/16

.... 361/770; 361/760; 361/767; 73; 361/774; 361/808; 174/260; 37; 257/738; 257/779; 257/780; 257/784; 257/786

..... 257/737-738, 31, 784, 786; 228/179.1, 180.1, 180.22; 29/876, 877, 878, 879; 61/760-774, 808; 174/260-261

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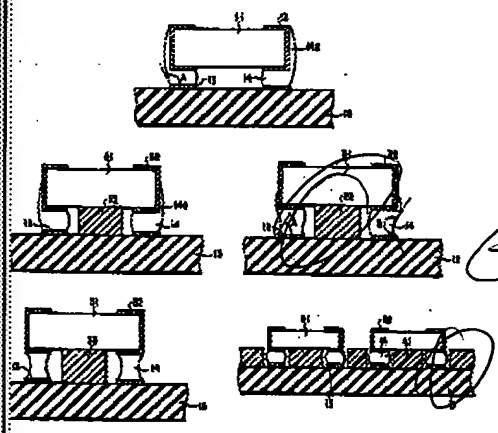
Primary Examiner—Bot L. Ledynh
Attorney, Agent, or Firm—Oblon, Spivak, McClelland, Maier & Neustadt, P.C.

[57] ABSTRACT

An electronic circuit device comprising a printed wiring board having a major surface and pads provided on the major surface of the printed wiring board, a plurality of electrodes provided partly on at least one major surface of the leadless component and partly on sides of the leadless component, a plurality of bumps provided on the pads, providing a gap between the major surface of the printed wiring board and the major surface of the leadless component, and electrically connecting those parts of the electrodes which are provided on the major surface of the leadless component to the pads, and a plurality of electrically conductive members integral with the bumps, extending from the bumps to those parts of the electrodes which are provided on the sides of the leadless component.

8 Claims, 9 Drawing Sheets



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Abstract Text - ABTX (1):

A method for testing an integrated circuit (IC) chip (10) in accordance with the invention comprises the step of forming a solder bump (14) on each of an array of bonding pads (13) on a first surface of the chip, in accordance with the known flip-chip method of IC device packaging. Each of the solder bumps (14) is inserted through an aperture (25) in a spacer member (22), the spacer member having a smaller thickness than the length of each solder bump, whereby each solder bump protrudes through an aperture. The solder bumps are then placed on a layer of anisotropic conductive material (11) which is arranged over an array of test fixture conductive pads so that the anisotropic conductive layer is sandwiched between the IC chip and the test fixture. The integrated circuit chip is then compressed against the anisotropic conductor material to establish electrical contact between the solder bumps of the integrated circuit chip and the test fixture conductor pads (17). The testing of the chip then proceeds by passing electrical current through the solder bumps, the anisotropic material, and the test fixture conductor pads in a known manner.

Application Filing Date - AD (1):

19911202

Brief Summary Text - BSTX (5):

The paper, "Flip-Chip Soldering to Bare Copper Circuits," by A. P. Ingraham et al., Proceedings of the Fortieth Electronic Components and Technology Conference, Las Vegas, Nev., pp. 333-337, May 1990, is an example of the prior art that describes a method for packaging and connecting integrated circuit chips known as flip-chip bonding or soldering. With this method, all terminals of the integrated circuit chip are located as conductor pads on one surface of the chip with a solder bump applied to each conductor pad. The chip is then mounted on a substrate with each solder bump contacting a conductor pad of the circuit to which it is to be connected. The apparatus is heated to reflow the solder and cause it to adhere to the

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US005206585A

United States Patent [19]

Chang et al.

[11] **Patent Number:**

[45] **Date of Patent:**

[54] **METHODS FOR TESTING INTEGRATED CIRCUIT DEVICES**

[75] Inventors: David D. C. Chang Edward L. Smith, Jr., both of Lawrenceville, N.J.

[73] Assignee: AT&T Bell Laboratories, Murray Hill, N.J.

[21] Appl. No.: 801,213

[22] Filed: Dec. 2, 1991

[51] Int. Cl.[5] G01R 1/073

[52] U.S. Cl. ..... 324/158 P; 324/72.5

[58] Field of Search ..... 324/158 P, 158 F, 72.5

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"Applications and Reliability of the AT&T Elastomeric Conductive Polymer Interconnection (ECPI) System", by J. A. Fulton et al., *Proceedings of the International Electronics Packaging Conference*, Mar 930-943, Sep. 1990.

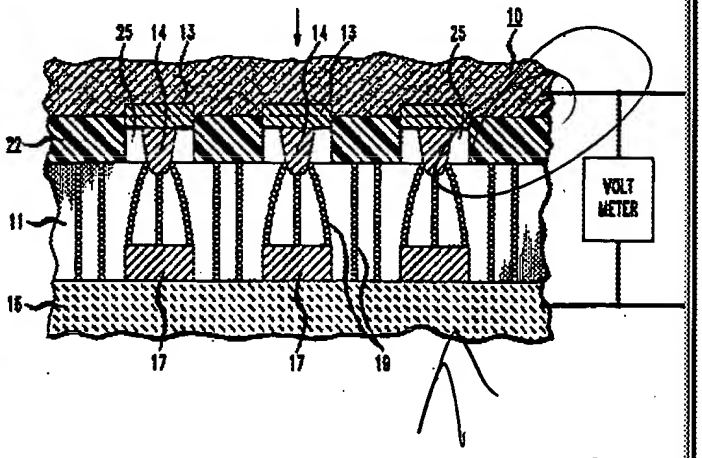
"Flip-Chip Soldering to Bare Copper P. Ingraham et al., *Proceedings of the F Components and Technology Confere* Nev., pp. 333-337, May 1990.

Primary Examiner—Ernest F. Karlsen *Attorney, Agent, or Firm*—R. B. Ande

[57] ABSTRACT

A method for testing an integrated circ in accordance with the invention com forming a solder bump (14) on each of ing pads (13) on a first surface of the ch with the known flip-chip method of IC ing. Each of the solder bumps (14) is an aperture (25) in a spacer member member having a smaller thickness th each solder bump, whereby each solde through an aperture. The solder bump on a layer of anisotropic conductive ma is arranged over an array of test fixture so that the anisotropic conductive lay between the IC chip and the test fixtur circuit chip is then compressed again conductor material to establish elect tween the solder bumps of the integr and the test fixture conductor pads (1 the chip then proceeds by passing through the solder bumps, the anisotro the test fixture conductor pads in a kn

8 Claims, 3 Drawing She



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